

Sheet 1 of 2

Form 1449*	Any. Docket No.: 303.678US4	Serial No. Unknown <i>09/943,393</i>
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Kie Y. Ahn et al.	
	Filing Date: Herewith	Group: Unknown <i>2818</i>

## U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
<i>PD</i>	5,668,035	09/16/1997	Fang, C.H., et al.	438	239	06/10/96
<i>↑</i>	5,985,725	11/16/1999	Chou, J.	438	294	12/23/97
<i>↓</i>	6,087,225	07/11/2000	Bronner, G.B., et al.	438	275	02/05/98
<i>↓</i>	6,097,056	08/01/2000	Hsu, L.L., et al.	257	315	04/28/98
<i>PD</i>	6,222,788	04/01/2001	Forbes, et al.	365	230.06	

## FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes 1 No
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## OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

<i>PD</i>	Chen, Y., et al., "Performance and Reliability Assessment of Dual-Gate CMOS Devices with Gate Oxide Grown Nitrogen Implanted Si Substrates", <u>International Electron Device Meeting</u> , pg. 1-4, (1997)
<i>↑</i>	Cho, I.H., et al., "Highly Reliable Dual Gate Oxide Fabrication by Reducing Wet Etching Time and Re-Oxidation for Sub-Quarter Micron CMOS Devices", <u>Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials</u> , pgs. 174-175, (1999)
<i>↓</i>	Crowder, S., et al., "Trade-offs in the Integration of High Performance Devices with Trench Capacitor DRAM", <u>Dig. Int. Electron Devices Meeting, Washington, D.C.</u> , pp. 45-48, (Dec. 1997)
<i>↓</i>	Fujiwara, M., et al., "New Optimization Guidelines for Sub-0.1 micrometer CMOS Technologies with 2 micrometer NO Gate Oxynitrides", <u>1999 Symposium on VLSI Technology Digest of Technical Papers</u> , pp. 121-122, (1999)
<i>↓</i>	Guo, X., et al., "High Quality Ultra-thin TiO <sub>2</sub> /Si <sub>3</sub> N <sub>4</sub> Gate Dielectric for Giga Scale MOS Technology", <u>Technical Digest of 1998 IEDM</u> , pp. 377-380, (1998)
<i>PD</i>	Han, L.K., et al., "Electrical Characteristics and Reliability of sub-3 nm Gate Oxides Grown on Nitrides Implanted Silicon Substrates", <u>Int. Electron Devices Meeting, Washington, D.C.</u> , pp. 1-4, (1997)

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\*Substitute Disclosure Statement form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Sheet 2 of 2

Form 1449*	Atty. Docket No.: 303.678US4	Serial No. <u>Unknown</u> 09/943,393
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## OTHER DOCUMENTS

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P D	Hideo, O., et al., "Dual Gate Oxide Process Integration for High Performance Embedded Memory Products", <u>Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials</u> , pp. 108-109, (1998)
	King, Y., et al., "Sub-5nm Multiple-Thickness Gate Oxide Technology Using Oxygen Implantation", <u>IEDM Technical Digest</u> , pp. 585-588, (1998)
	Liu, C.T., et al., "Multiple Gate Oxide Thickness for 2GHz System-on-A-Chip Technologies", <u>IEDM Technical Digest</u> , pp. 589-592, (1998)
	Ma, T.P., "Making Silicon Nitride film a Viable Gate Dielectric", <u>IEEE Trans. On Electron Devices</u> , 45(3), pp. 680-690, (1998)
	Muller, D.A., et al., "The Electronic Structure at the Atomic Scale of Ultrathin Gate Oxides", <u>Nature</u> , 399, 758-761, (June 1999)
	Oi, H., et al., "Dual Gate Oxide Process Integration for High Performance Embedded Memory Products", <u>Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials</u> , pp. 108-109, (1998)
	Saito, Y., et al., "High-Integrity Silicon Oxide Grown at Low-temperature by Atomic Oxygen Generated in High-Density Krypton Plasma", <u>Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials</u> , pp. 152-153, (1999)
	Togo, M., et al., "Multiple-Thickness Gate Oxide and Dual-Gate Technologies for High Performance Logic-Embedded DRAMs", <u>IEDM Technical Digest</u> , pp. 347-350, (1998)
P D	Tseng, H., et al., "Application of JVD Nitride Gate Dielectric to A 0.35 Micron CMOS Process for Reduction of Gate Leakage Current And Boron Penetration", <u>Int. Electron Device Meeting</u> , San Francisco, CA, pp. 1-4, (1998)

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